FUSE DENSITY ON AN INKJET PRINTHEAD CHIP

BACKGROUND OF THE INVENTION

[0001] The present invention relates to inkjet printers, and particularly to memory on the heater chip of an inkjet printhead.

[0002] An inkjet printhead generally has a heater chip. The heater chip typically includes logic circuitry, a plurality of power transistors, and a set of heaters or resistors. A hardware or software printer driver will selectively address or energize the logic circuitry such that appropriate resistors are heated for printing. The memory is also used to identify the printhead to determine if the printhead is a monochrome printhead, a color printhead or a photograph quality printer printhead.

[0003] In the fuse configuration, the memory is an array of fuse memory elements. Each fuse memory element has a unique power transistor to enable writing or reading. This type of fuse memory has a constant memory density, for example, 140 bits per square millimeter. For example, a set of 13 fuses and programming transistors in an area 280 μm x 340 μm (95200 μm^2) yields 7323 μm^2 per fuse, which is 137 fuses per 1,000,000 μm^2 (or 1 mm^2). Typical read currents are less than 5 mA; typical write or programming current is greater than 50 mA. Power transistors capable of generating the required programming current typically occupy a very large area per fuse. As a result, the number of memory elements is limited depending upon printhead size.

SUMMARY OF THE INVENTION

[0004] Accordingly, there is a need for an improved memory for a printhead. In one form, the present invention provides a programmable memory on an inkjet printhead chip. The memory comprises a memory array that has a plurality of memory elements. The memory also comprises a bipolar device that isolates a /memory element from another memory element in the memory array.

[0005] In another form, the present invention provides a programmable memory on an inkjet printhead chip. The memory comprises a memory array that has a plurality of circuit elements arranged in rows and a plurality of circuit elements arranged in columns. The columns intersect the rows to thereby form a plurality of memory elements. The memory also includes a bipolar element that is coupled to the memory element and that is configured to isolate the memory element from another memory element.

[0006] In yet another form, the present invention provides a method of providing high fuse density in a printhead heater chip. The method comprises the acts of arranging a plurality of memory elements in a memory array, and isolating a memory element from another memory element in the memory array with a bipolar device.

[0007] Other features and advantages of the invention will become apparent to those skilled in the art upon review of the following detailed description, claims, and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] In the drawings:

[0009] FIG. 1 illustrates an inkjet printhead according to one embodiment of the present invention;

[0010] FIG. 2 shows a fuse-diode matrix arrangement of one embodiment of the present invention

[0011] FIG. 3 shows a basic fuse configuration;

[0012] FIG. 4 shows a graph comparing fuse densities obtained from the arrangements in FIGS. 2 and 3;

[0013] FIG. 5 shows a sectional view of a portion of the arrangement in FIG. 2 according to one embodiment of the invention;

[0014] FIG. 6 shows a top view of the portion of the arrangement in FIG. 5 according to one embodiment of the invention;

[0015] FIG. 7 shows a top view of a portion of the arrangement in FIG. 5 with a p-type surrounding guard ring according to the present invention;

[0016] FIG. 8 shows a top view of a portion of the arrangement in FIG. 5 with a n-type surrounding guard ring according to the present invention; and

[0017] FIG. 9 shows a top view of a portion of the arrangement in FIG. 5 with a common surrounding guard ring according to the present invention.

[0018] Before any embodiments of the invention are explained in detail, it is to be understood that the invention is not limited in its application to the details of construction and the arrangement of components set forth in the following description or illustrated in the following drawings. The invention is capable of other embodiments and of being practiced or of being carried out in various ways. Also, it is to be understood that the phraseology and terminology used herein is for the purpose of description and should not be regarded as limiting. The use of "including," "comprising," or "having" and variations thereof herein is meant to encompass the items listed thereafter and equivalents thereof as well as additional items. Unless limited otherwise, the terms "connected," "coupled," and "mounted" and variations thereof herein are used broadly and encompass direct and indirect connections, couplings, and mountings. In addition, the terms "connected" and "coupled" and variations thereof are not restricted to physical or mechanical connections or couplings.

DETAILED DESCRIPTION

[0019] FIG. 1 illustrates an inkjet printhead 10 according to one embodiment of the present invention. The printhead 10 includes a housing 12 that defines a nosepiece 13 and an ink reservoir 14 containing ink or a foam insert saturated with ink. The housing 12 can be constructed of a variety of materials including, without limitation, at least one of polymers, metals, ceramics, composites, and the like. The

inkjet printhead 10 illustrated in FIG. 1 has been inverted to illustrate a nozzle portion 15 of the printhead 10. The nozzle portion 15 is located at least partially on a bottom surface 11 of the nosepiece 13 for transferring ink from the ink reservoir 14 onto a printing medium. The nozzle portion 15 can include a heater chip 16 (not visible in FIG. 1) and a nozzle plate 20 having a plurality of nozzles 22 that define a nozzle arrangement and from which ink drops are ejected onto printing medium that is advanced through a printer (not shown). The nozzles 22 can have any cross-sectional shape desired including, without limitation, circular, elliptical, square, rectangular, and any other polygonal shape that allows ink to be transferred from the printhead 10 to a printing medium. The heater chip 16 can be formed of a variety of materials including, without limitation, various forms of doped or non-doped silicon, doped or non-doped germanium, or any other semiconducting material. The heater chip 16 is positioned to be in electrical communication with conductive traces 17 provided on an underside of a tape member 18.

[0020] The heater chip 16 is hidden from view in the assembled printhead 10 illustrated in FIG. 1 and is attached to the nozzle plate 20 in a removed area or cutout portion 19 of the tape member 18 such that an outwardly facing surface 21 of the nozzle plate 20 is generally flush with and parallel to an outer surface 29 of the tape member 18 for directing ink onto a printing medium via the plurality of nozzles 22 in fluid communication with the ink reservoir 14.

[0021] FIG. 2 shows a portion of a fuse-bipolar matrix memory arrangement or a programmable memory array 100 positioned in the heater chip 16 arranged according to the present invention. Specifically, the portion shown in FIG. 2 is from a 128 bytes by 8 bits array, that is, the array has a total of 1024 fuses. . Although only a portion of the array of fuses is shown (as a 3x3 array), other fuse numbers can be achieved by the present invention. Furthermore, a floating gate can also be used in place of the fuse 104 in other embodiments. The fuse element 104 can be a tantalum aluminum (TaAl) filament, a tantalum aluminum nitride (TaAlN) filament, and the like. The heater chip 16 can also have a plurality of heater layers depending on the application.

[0022] The memory array 100 has a plurality of bipolar devices 108 such as diodes, pnp transistors, or npn transistors. The bipolar devices 108 are used to isolate each fuse 104 so that a transistor can be used to program or read many different fuses based on the address sent from a printer. Specifically, a plurality of row programming transistors 112, and a plurality of column programming transistors 116 form the array of memory elements. The memory 100 can be programmed by selecting the row power transistor 112 and a corresponding column 116. Having the row transistors and the column transistors thus reduces areas covering the fuse 104 and the bipolar device 108. As a result, overall area of the array 100 can be greatly reduced or the number of memory elements can be increased in a same amount of chip area.

[0023] When compared to a basic fuse configuration 200 as shown in FIG. 3, the basic fuse configuration 200 requires a programming transistor 204 for each memory element. For example, printhead model HP57 of Hewlett Packard uses 13 fuses and 13 programming transistors in an area 280 μm x 340 μm, or 95200 μm^2. In other words, the HP57 printhead has a fuse density of 95200 μm^2/13 fuses, or 7323 μm^2 per fuse, which is approximately 1,000,000 μm^2/7323 μm^2 or 137 fuses per 1,000,000 μm^2 (or 1 mm^2). Furthermore, there are two groups of these fuses on the HP57 for a total of 26 fuses on the chip. The memory arrangement 100 in FIG. 2, on the other hand, only requires a programming transistor 116 for each bit and byte rows.

[0024] In other words, due to the fact that a power transistor occupies relatively larger area, the relatively smaller area occupied by a bipolar device allows the memory array 100 to be relatively smaller in size. As shown in FIG. 4, the memory density obtained with the basic fuse configuration 200 is a generally constant curve 304. On the other hand, as the array 100 or number of bits increases, the corresponding memory density or bits per square millimeter increases (curve 308) as shown in FIG. 4. For example, a 2x8 array of 16 bits has a memory density of at least 200 bits per square millimeter. In another example, an array of 200 bits has a memory density of at least 700 bits per square millimeter using the array configuration in FIG. 2. In contrast, 140 bits per square millimeter is obtained regardless of the number of bits used with the array configuration in FIG. 3.

[0025] FIGS. 5 and 6 show a sectional view and a top view, respectively, of a portion of the memory arrangement 100. As shown in FIG. 5, a bit column programming transistor 116 is coupled to a p-type emitter 158, and a byte row programming transistor 112 is coupled to an n-type base 162. When both the bit programming transistor 116 and the byte programming transistor 112 are activated to write to fuse 170, a parasitic effect or latch up condition may occur. For example, a parasitic vertical pnp device 166 will be formed by a second fuse 174 and a parasitic lateral NPN device 178. The parasitic vertical pnp device 166 may be turned on when the transistors 112, 116 are activated. The latch up condition will cause fuse 174 to be programmed unintentionally. As a result, in order to achieve high density memory using the memory array arrangement 100, the bipolar devices 108 such as pnp devices are also isolated to prevent the latch up condition.

[0026] To prevent the latch up condition described above, the bipolar devices 108 are generally isolated with a surrounding guard ring as shown in FIGS. 7, and 8. Specifically, a p-type surrounding guard ring 304 is connected to a ground rail 308. The p-type surrounding guard ring 304 is also positioned around each of the bipolar devices 108 in FIG. 7. In this way, the ground connected p-type surrounding guard ring 304 will provide a current drainage through the ground rail 308 for the parasitic currents. Similarly, an n-type surrounding guard ring 312 is connected to a voltage rail 316 that provides high potentials, as shown in FIG. 8. The n-type surrounding guard ring 312 is also positioned around each of the bipolar devices 108. Thus, the voltage rail connected n-type guard ring 312 will also provide a current drainage through an n-type base of the surrounding guard ring 312.

[0027] In another embodiment, the latch up condition can also be prevented by having a common device type between the bipolar devices 108. As shown in FIG. 9, each bipolar device 108 has an n-well 320 encompassing both the p-type emitter 158 and the n-type base 162. The n-well 320 of the bipolar device 108 is joined with the n-well 320 of an adjacent bipolar device 108 that is connected to the same row programming transistor 112. FIG. 9 also shows that the latch up condition can also be prevented by a p-type isolation 324 connected to the ground rail 308. In yet another

embodiment, an n-type isolation can be connected to the voltage rail 316 that provides high potentials.

[0028] Various features and advantages of the invention are set forth in the following claims.